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REMARKS

Claims 11-20 and 22-34 are pending in this application. By this Amendment, Applicants amend Claims 11-15, 20, and 22-26, cancel claims 10 and 21, and add claims 27-34.

The Examiner indicated that each page of the drawings, declaration, claims, specification and abstract have a line from the top of each page to the bottom of each page, and that Applicants are required to correct the line before the present application is issued for allowance. Applicants submit herewith copies of the above-identified documents which do not include the line from the top of each page to the bottom of each page.

The Examiner's indication that claims 14, 15 and 23 would be allowable if rewritten in independent form including all of the features of the base claim and any intervening claims is appreciated.

Claims 10-13, 16-18, 20-22, 24 and 26 were rejected under 35 U.S.C. § 102(b) as being anticipated by Troeller et al. (U.S. 5,768,445). And claims 19 and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Troeller et al. in view of Schilling et al. (U.S. 6,236,405).

Applicants have amended allowable claims 14, 15 and 23 to be independent and to include all of the features of the base claim.

In view of the foregoing, Applicant respectfully submits that claims 14, 15 and 23 are allowable. Claims 11-14 and 16-20 and claims 22 and 24-26 are dependent upon claims 14 and 23, respectively, and are therefore allowable for at least the reasons that claims 14 and 23 are allowable.

In view of the foregoing Amendments and Remarks, Applicant respectfully submits that this Application is in condition for allowance. Favorable consideration and prompt allowance are respectfully solicited.

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The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

Date: June 10, 2002

Attorneys for Applicant

Joseph R. Keating
Registration No. 37,368

Christopher A. Bennett
Registration No. 46,710

KEATING & BENNETT LLP
10400 Eaton Place, Suite 312
Fairfax, VA 22030
Telephone: (703) 385-5200
Facsimile: (703) 385-5080

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

11. The apparatus of claim [10] 14, further comprising a frame buffer, wherein said processor stores image data in said frame buffer.

12. The apparatus of claim [10] 14, wherein said processor reads decompressed texture data contained in said texture buffer and performs image processing of said decompressed texture data for conversion to image data.

13. The apparatus of claim [10] 14, wherein said processor reads compressed texture data from said first storage device, said data decompression circuit decompresses said read compressed texture data, and said processor stores said decompressed texture data in said texture buffer.

14. [The] An apparatus [of claim 10,] for image processing, comprising:
a processor including a data decompression circuit;
a first storage device having texture data and electronically coupled to said processor; and
a texture buffer having decompressed texture data and electrically coupled to said processor; wherein
transmission of texture data between said texture buffer and said processor is faster than transmission of texture data between said storage device and said processor.

15. [The] An apparatus [of claim 10,] for image processing, comprising:
a processor including a data decompression circuit;
a first storage device having texture data and electronically coupled to said processor;
a texture buffer having decompressed texture data and electrically coupled to said processor; and [further comprising]

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a first data bus and a second data bus, wherein said first data bus carries texture data between said texture buffer and said processor faster than said second data bus carries texture data from said storage device and said processor.

20. The apparatus of claim [10] <u>14</u>, wherein said texture data in said first storage device is compressed.

22. The method of claim [21] <u>23</u>, further comprising the step of converting said decompressed texture data to image data, and storing said image data in a frame buffer.

23. [The] <u>An image processing</u> method [of claim 21, further] comprising <u>the steps of:</u>
<u>providing compressed texture data in a storage device;</u>
<u>reading said compressed texture data from said storage device and</u>
<u>decompressing said compressed texture data;</u>
<u>storing said decompressed texture data in a texture buffer; and</u>
[the step of] providing a processor, and transferring data between said texture buffer and said processor faster than transferring data between said storage device and said processor.

24. The method of claim [21] <u>23</u>, further comprising the step of performing palette conversion of said decompressed texture data prior to said step of storing said texture data.

25. The method of Claim [21] <u>23</u>, further comprising the step of generating a mip map of said compressed texture data prior to said step of storing said decompressed texture data.

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26. The method of claim [21] 23, wherein said step of storing said decompressed texture data includes the step of updating said decompressed texture data in said texture buffer with new decompressed texture data.